

FIG. 1

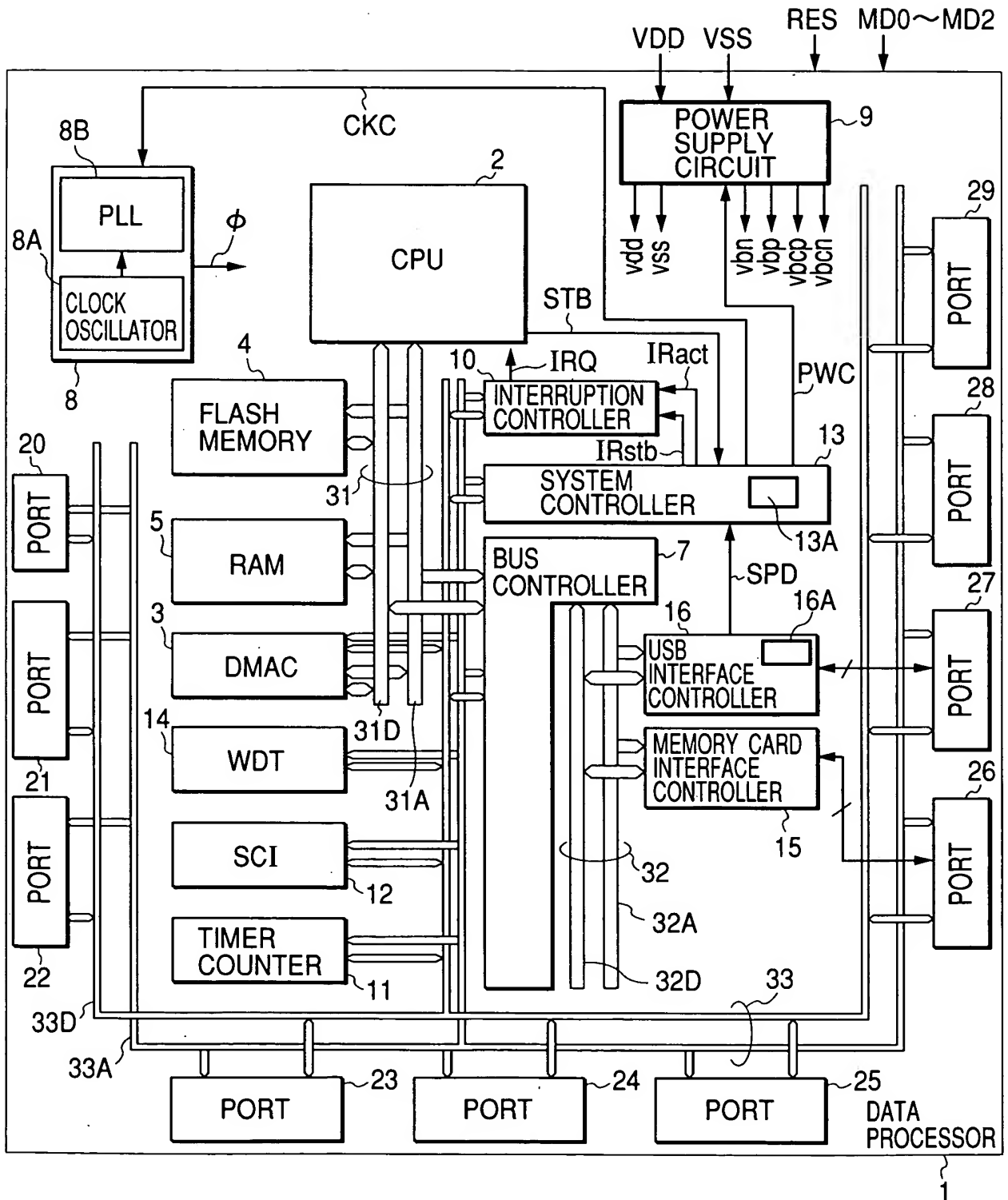


FIG. 2

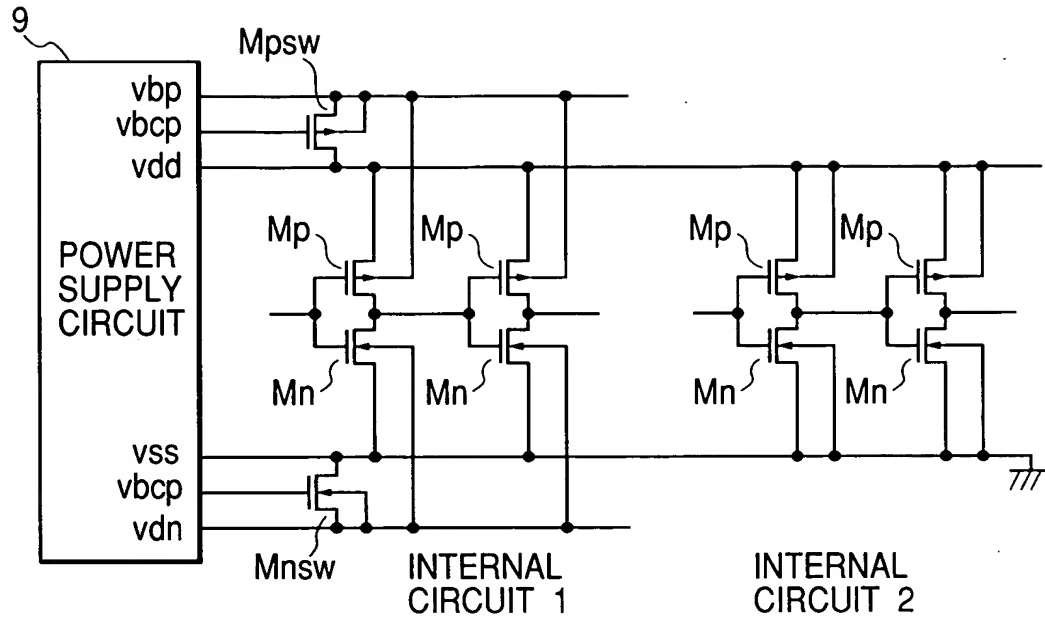


FIG. 3

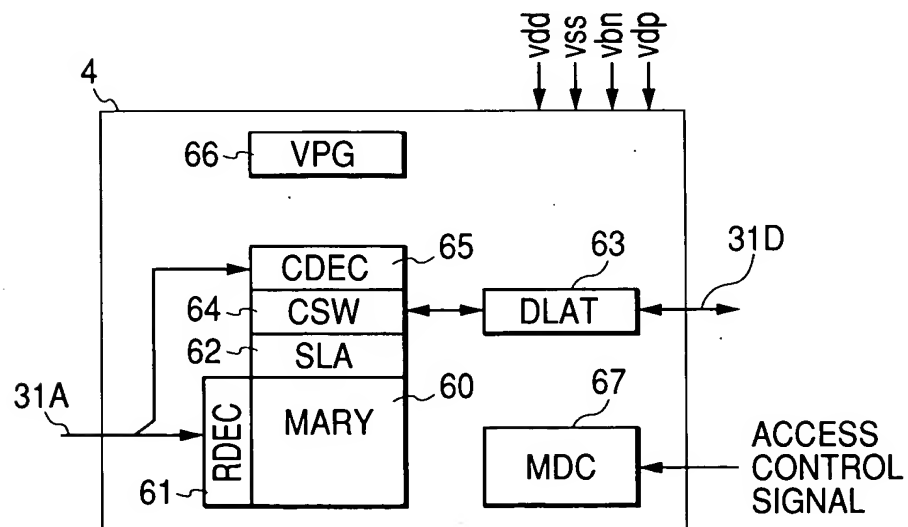


FIG. 4

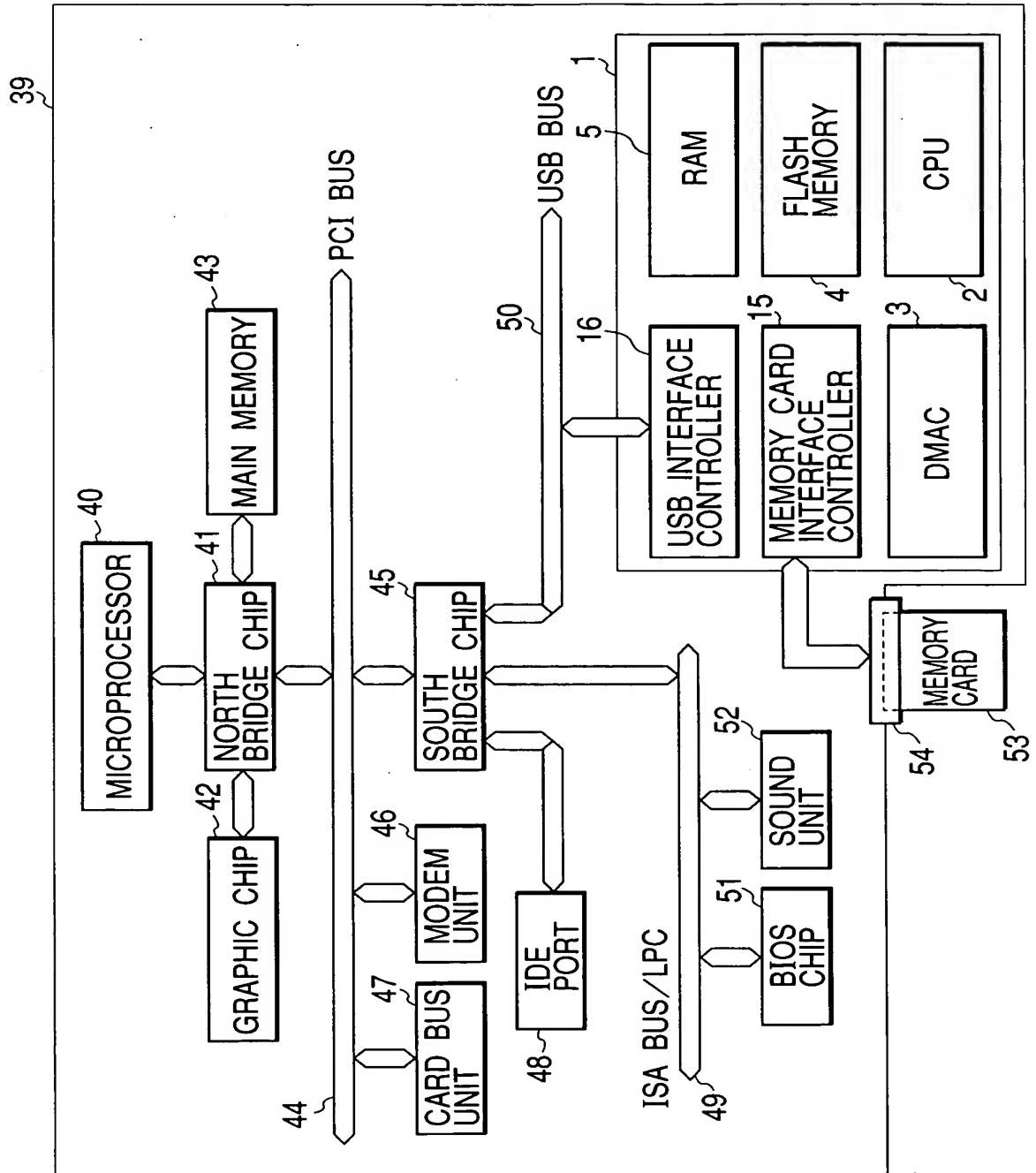


FIG. 6

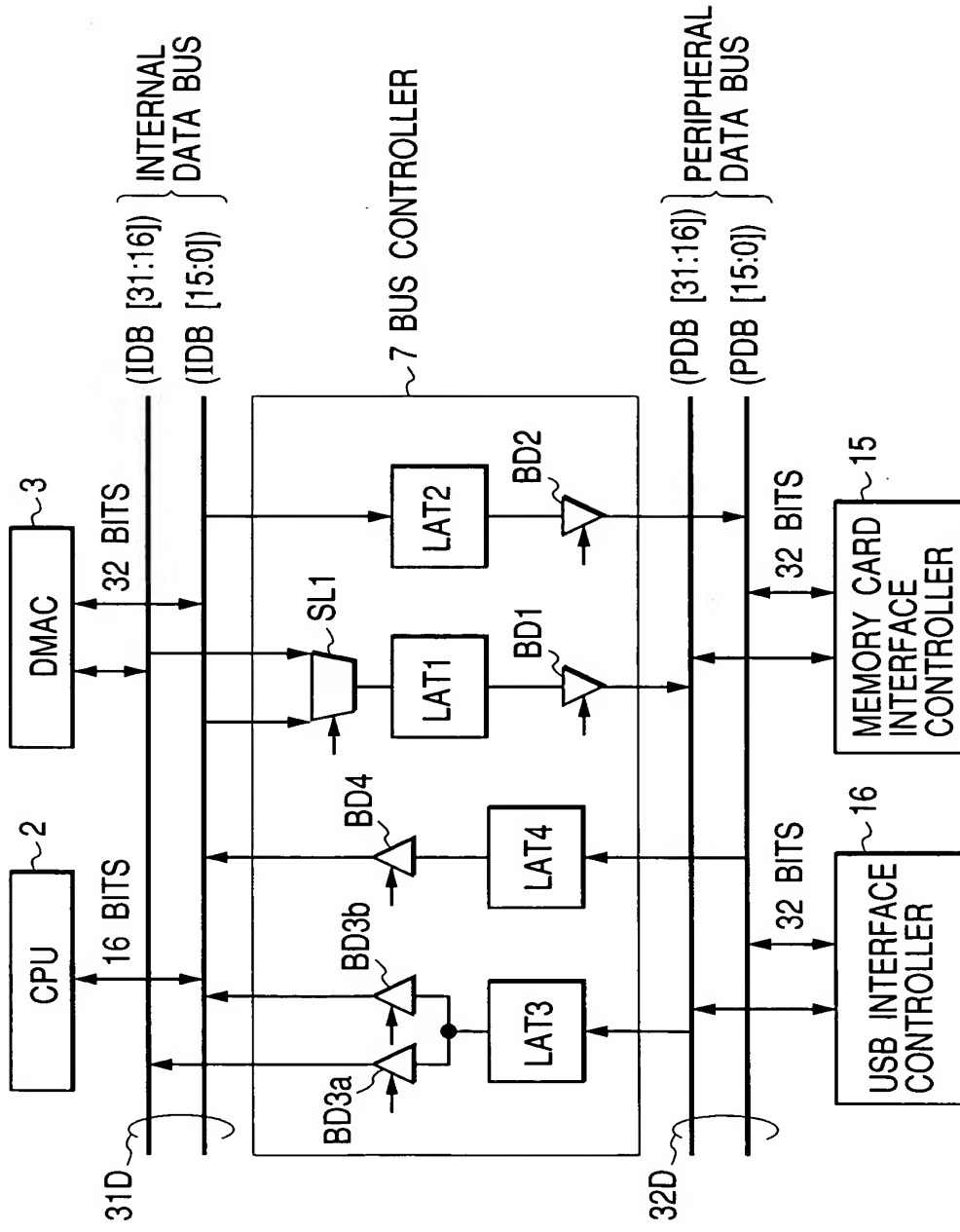


FIG. 7

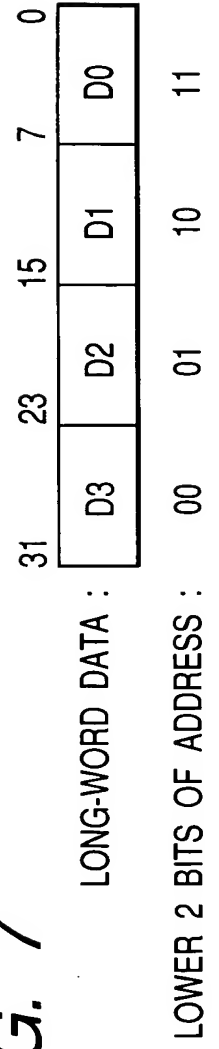


FIG. 8

	ADDRESS	DATA				CPU	DMAC
	1, 0	31	23	15	7..0		
LONG-WORD	xx	D3	D2	D1	D0	×	○
WORD	0x	—	—	D3	D2	○	○
	1x	—	—	D1	D0	○	○
BYTE	00	—	—	D3	—	○	○
	01	—	—	—	D2	○	○
	10	—	—	D1	—	○	○
	11	—	—	—	D0	○	○

FIG. 9

	ADDRESS	DATA			
	1, 0	31	23	15	7..0
LONG-WORD	xx	D3	D2	D1	D0
WORD	0x	D3	D2	—	—
	1x	—	—	D1	D0
BYTE	00	D3	—	—	—
	01	—	D2	—	—
	10	—	—	D1	—
	11	—	—	—	D0

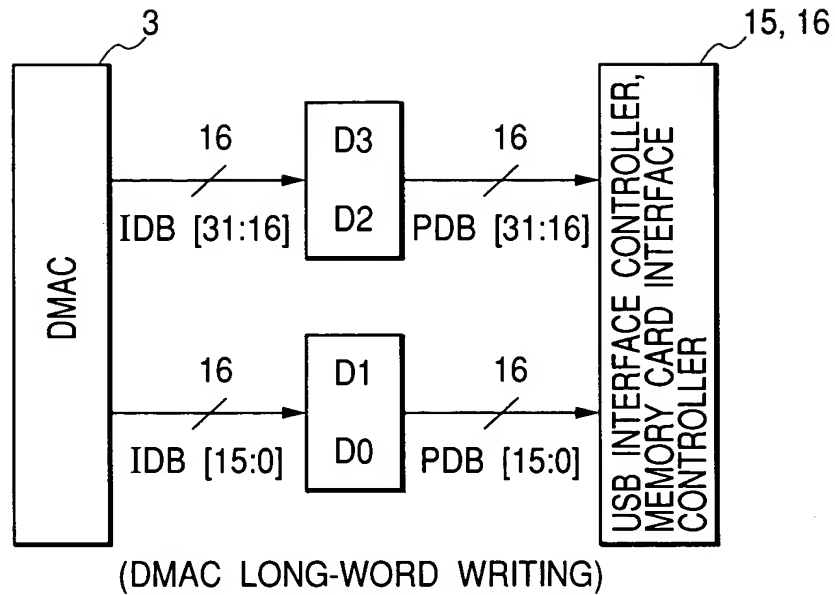
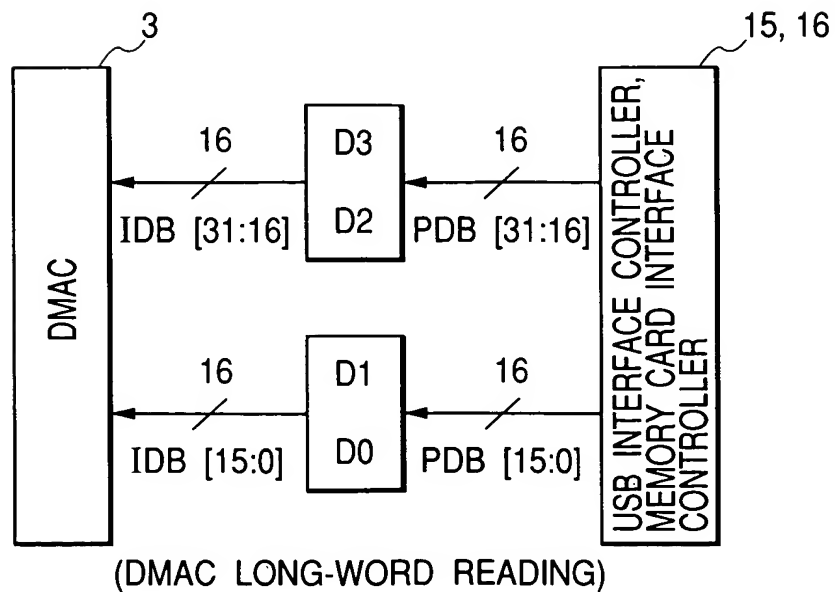
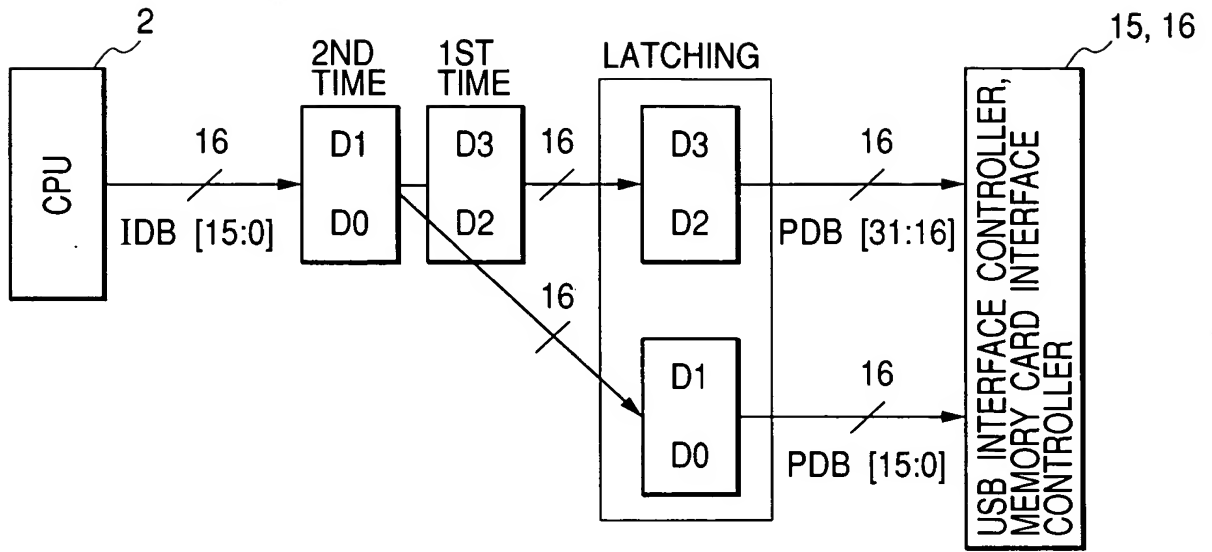
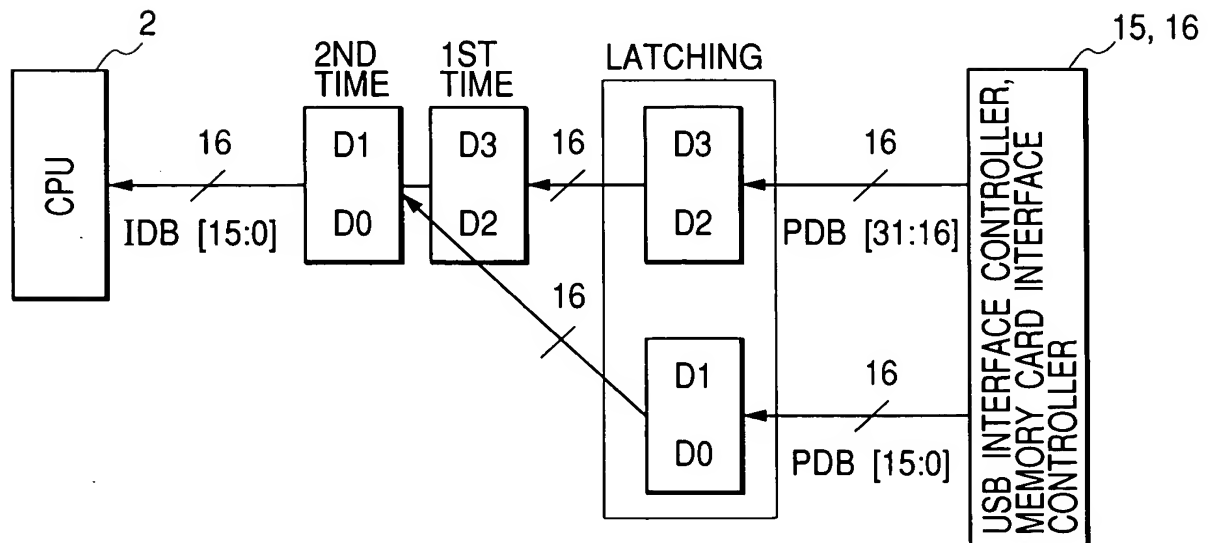
FIG. 10**FIG. 11**

FIG. 12

(CPU LONG-WORD WRITING)

FIG. 13

(CPU LONG-WORD READING)

FIG. 14